

ABSTRACT

Power wastefully consumed in a memory in standby state is reduced without lowering the speed of operation of reading data out of the memory. A semiconductor integrated circuit has a memory which can enter active state or standby state, and the memory has voltage generation circuits for bit lines and source lines with which memory cells are connected. The voltage generation circuits make the potential of the bit lines and the potential of the source lines equal to each other in response to an instruction to transition from active state to standby state. The voltage generation circuits produce a potential difference between the bit lines and the source lines in response to an instruction to transition from standby state to active state. In standby state, the potential of the bit lines and that of the source lines are equal to each other. Therefore, sub-threshold leakage does not occur between the source and drain of each memory cell. In active state, the source line potential is not varied. Therefore, the speed of data readout operation is not lowered.